Amendments to the Specification:

Please replace the fourth paragraph beginning on page 2 and continuing to page 3 with the following amended paragraph:

FIG. 1a is a schematic illustration of a damascene connector. Seen there is an FSG layer 12 on a substrate 11. Via hole 31 was etched through the full thickness of layer 12 so as to expose substrate 11 which, in most cases, would be the upper surface of a partially formed integrated circuit, and then just filled with copper material [[31]]44 (after laying down barrier layer 14). The filling step is accomplished by initially over-filling with copper and then removing the excess by means of chemical mechanical polishing (CMP).